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リアルタイム最適制御に基づくVLSIプロセッサの低電力化

Low-Power VLSI Processor Based on Real-Time Optimal Control

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1. Introduction

In the recent deep-submicron era, fluctuation exists in transistor parameters in a dynamic manner. Complexity of power supply line in VLSI processors is increased because of larger number of transistors in a single chip. Consequently, on-chip supply voltage fluctuation becomes remarkable due to IR-drop and fluctuation caused by inductances as shown in Eqs. (1) and (2) and Fig.1. Let V_{DD} be a real supply voltage superposed by fluctuation, and let V_d be a desired supply voltage.

$$V_{DD} = V_d + \Delta V \tag{1}$$

$$\Delta V = IR + L\frac{di}{dt} \tag{2}$$

Large voltage drop due to metal resistance exists when large current flows through power supply line. This deviation might vary space-by-space and time-by-time in VLSI processors. Because of this fluctuation, power consumption and circuit delay will vary, hence affecting the circuit performance. For an example, ±0.2V supply voltage fluctuation may cause almost 15% of delay and even cause the circuit to function incorrectly. There is performance limitation due to a fixed control, where a transistor threshold voltage V_{TH} is fixed during real-time operations. By using a variable threshold voltage, leakage power consumption is greatly reduced with maintaining the circuit speed.

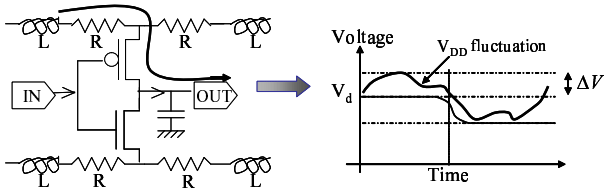

Fig. 1 Supply voltage fluctuation

The leakage power and frequency in a chip can

be controlled to some extent using body bias to modulate the threshold voltage of a transistor[1]. There are two ways in controlling V_{TH}. They are reverse body bias (RBB)[2] and forward body bias (FBB)[3]. RBB has been used to reduce leakage current consumption effectively by increasing the body-bias voltage of a pMOS transistor to be larger than a supply voltage. For an nMOS transistor, the body-bias voltage is reduced to be lower than ground. These changes cause V_{TH} increased during standby mode. FBB is used during active mode to decrease V_{TH} and improving circuit performance although it increases leakage power consumption. Both of these techniques, RBB and FBB are popularly used to control V_{TH} and to realize a variable threshold-voltage scheme in CMOS transistors. Figure 2 shows an example how body-bias voltage has effects on a threshold voltage under RBB and FBB.

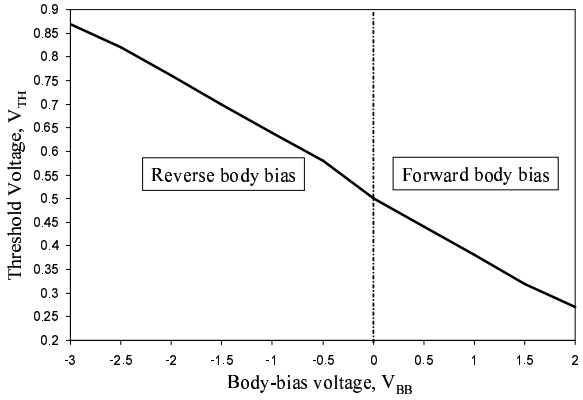

Fig. 2 Effect of body-bias on a threshold voltage

2. Adaptive Threshold Voltage

Generally, the bulk voltage of the conventional CMOS logic circuit is connected to V_{DD} for the case of a pMOS transistor and to the ground for the case of an nMOS transistor. It is well known that the pMOS and the nMOS body-bias control is useful in changing V_{TH} and for subthreshold leakage current minimization. To retain the correct operation due to fluctuation, real-time adaptive threshold voltage control (ATVC) is introduced to minimize power consumption under a time constraint. In this case, internal states of a module should be easily detected, that is, observability is important as well as controllability as shown in Fig.3.

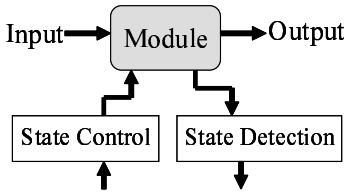

Fig. 3 Basic adaptive control architecture

2.1 Adaptive Threshold Voltage Control (ATVC) Scheme

Since supply voltage V_{DD} fluctuation varies higher and lower than a desired supply voltage V_d, so RBB and FBB can be effectively used to control a transistor threshold voltage, adaptively. From the Eqs. (3) and (4), power consumption is small if V_{DD} is low, while the delay becomes large. V_{TH} has to be decreased to retain the speed. When V_{DD} is high, the higher V_{TH} reduces the leakage current under the same delay condition and thus minimize the power consumption. Basically, by raising V_{TH} when a supply voltage fluctuates above V_d, it minimizes the power consumption. Besides that, by lowering V_{TH} when a supply voltage fluctuates below V_d, it improves circuit performance.

$$\text{Power, P} = (\mathrm{p}_t \mathrm{C} \mathrm{V}_{DD}{}^2 + \int \mathrm{i}_{dp} \mathrm{dt} \mathrm{V}_{DD}) \mathrm{f}_{clk} + I_{leak} V_{DD} 10^{-V_{TH}/S} \quad (3)$$

$$Delay, t_d = \frac{(k * C * V_{DD})}{(V_{DD} - V_{TH})^{\alpha}} \quad (4)$$

From the above equation, the leakage current(I_{leak}) is inversely proportional to V_{TH} as written in Eq. (5).

$$I_{leak} \alpha exp(-V_{TH}) \tag{5}$$

ATVC allows each bulk of CMOS transistors to have optimum V_{TH} in order to reduce the effects of fluctuation. Figure 4 shows a module whose V_{TH} value can be controlled by a control circuit. The ATVC scheme selects an appropriate body-bias voltage with respect to the changes in V_{DD}. The same V_{DD} used in the module, is also used for a control circuit. V_{DD} is compared with several reference voltages in a control circuit. If the fluctuated V_{DD} is higher than a desired supply voltage, control circuit selects higher V_{TH}. While the fluctuated V_{DD} is lower than a desired supply voltage, control circuit selects lower V_{TH}.

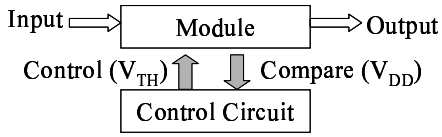

Fig. 4 ATVC architecture

In this paper, the control frequency is assumed to be higher than the supply voltage fluctuation frequency. This assumption is important because this allows sufficient time for the appropriate body-bias voltage to be selected and for the bulk CMOS to adapt to the new threshold voltage before the control circuit updates a new voltage fluctuation.

2.2 Optimal Control Algorithm

It is important to find a simple control algorithm in designing a simple control circuit. Let V_{DD} fluctuation be 1.8V±10% or 1.8V±0.2V. Therefore it varies from 1.6V to 2.0V. Under this condition, 5 levels of reference voltages are considered. If more voltage references and wider range of V_{DD} fluctuation are considered, power reduction ratio will become larger.

An optimal V_{TH} for each case of V_{DD} fluctuation is chosen if it satisfies a time constraint, T and power minimization. Each of this optimal V_{TH} is then selected adaptively based on the range of supply voltage fluctuation during real-time operations. Supply voltage 1.8V is chosen as a desired supply voltage V_d and it acts like a starting point. At that voltage, there is no deviation and it is the normal condition. The substrate bias voltage V_{SB} is zero and V_{TH} is set to V_{TH3}. The delay time t_d when supply voltage is V_d and threshold voltage is V_{TH3}, becomes the time constraint T. Incorrect value of a time constraint causes inaccurate value of optimal V_{TH}.

We assumed V_{TH} for a pMOS transistor is same with V_{TH} for an nMOS transistor. Figure 5 shows an example of an inverter using ATVC scheme based on an optimal control algorithm. In real-time, optimal V_{TH} is obtained by the following algorithm where $V_{TH1} > V_{TH2} > V_{TH3} > V_{TH4} > V_{TH5}$.

V_{TH}=V_{TH1}; If (V_{TH1},V_{TH2},V_{TH3},V_{TH4} and V_{TH5})
satisfy t_d=g(V_{DD},V_{TH})≦T
V_{TH}=V_{TH2}; If (V_{TH2},V_{TH3},V_{TH4} and V_{TH5})
satisfy t_d=g(V_{DD},V_{TH})≦T
V_{TH}=V_{TH3}; If (V_{TH3},V_{TH4} and V_{TH5})
satisfy t_d=g(V_{DD},V_{TH})≦T
V_{TH}=V_{TH4}; If (V_{TH4} and V_{TH5})
satisfy t_d=g(V_{DD},V_{TH})≦T
Otherwise V_{TH}=V_{TH5}

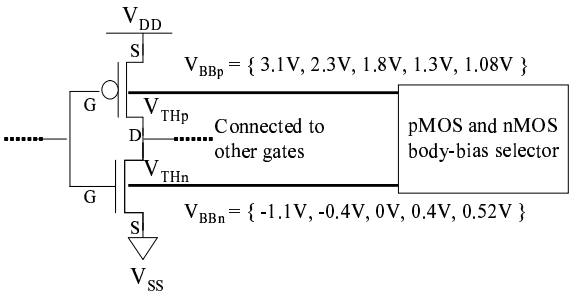

Fig. 5 ATVC based on an optimal control

3. Optimal Control Circuit

A control circuit is designed to be as simple as possible but there are still area and power consumption overhead caused by a control circuit. To overcome area and power consumption overhead, targeted module should contain many transistors such as 100 NAND gates. A control circuit consists of a voltage comparator and a voltage selector. Figure 6 shows the schematic diagram of ATVC scheme. V_{DD} fluctuation is compared in a voltage comparator and the output becomes the input of a voltage selector. A voltage selector is introduced to select an appropriate body-bias voltage. Output from a voltage comparator enable transistors in a voltage selector and the selected voltage becomes pMOS and nMOS body-bias voltage. Each body-bias voltage represents different values of threshold voltage.

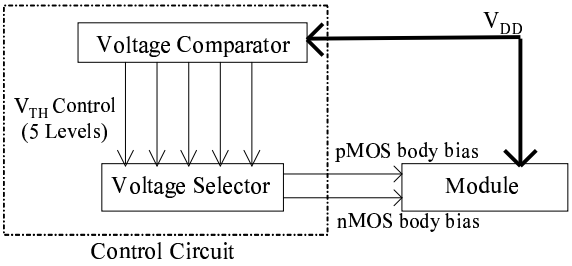

Fig. 6 Schematic diagram of the ATVC scheme

4. Simulation

For an example, an inverter is chosen as the targeted module. Using 0.18μm CMOS standard design rule, ATVC is verified on HSPICE simulation. Power consumption and delay time dependency on V_{DD} and V_{TH} are simulated and their relationship is analyzed. V_{TH} that is selected is an optimal one as it meets a time constraint and is used for a range of V_{DD} as shown in Eq. (6). Value x and y are the minimum and maximum supply voltage, respectively for an optimal V_{TH}. In this case a time constraint T is fixed at 29.2ps as shown in Fig.7.

$$V_{THi}(i = 1, 2, 3, 4, 5) \Rightarrow x_i \leqq V_{DD} \leqq y_i \quad (6)$$

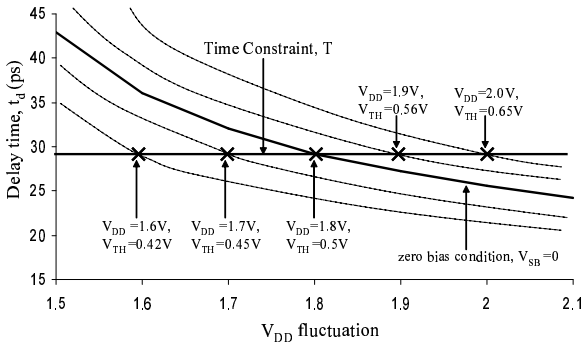

Fig. 7 Delay time dependency on V_{DD} and V_{TH}

5. Evaluation

Table 1 shows delay time, power and leakage current when V_{DD} fluctuation occurs but V_{TH} remains unchanged. It means that at this time no threshold voltage control is applied. Table 2 shows delay time, power and leakage current after ATVC scheme is applied. We can see that when V_{DD} fluctuates above a desired voltage which is 1.8V, power is reduced at average of 2% and leakage current is reduced at average of 35%. However, when V_{DD} fluctuates below a desired voltage, decreasing V_{TH} is necessary to maintain the circuit performance under delay time consideration although

it increases power consumption especially leakage power.

V_{DD} [V]	V_{TH} [V]	Delay, t_d [ps]	Power [μw]	Leakage Current [A]
2.0	0.50	25.6	3.324	2.01p
1.9	0.50	27.3	2.979	1.91p
1.8	0.50	29.2	2.636	1.81p
1.7	0.50	32.0	2.311	1.71p
1.6	0.50	36.0	2.036	1.61p

Table 1 Delay time, power and leakage current without ATVC scheme

V_{DD} [V]	V_{TH} [V]	Delay, t_d [ps]	Power [μw]	Leakage Current [A]
2.0	0.65	29.1	3.234	0.89p
1.9	0.56	29.0	2.944	1.49p
1.8	0.50	29.2	2.636	1.81p
1.7	0.45	29.0	2.377	57.8n
1.6	0.42	29.1	4.665	6.17u

Table 2 Delay time, power and leakage current with ATVC scheme

6. Conclusion

Real-time adaptive threshold voltage control scheme using body-bias control is effective in changing V_{TH} to minimize leakage power as well as to improve circuit performance under a time constraint. Further study should be done to implement a complete control circuit in real-time. In addition, real-time optimal control scheme can be employed to compensate variation in threshold voltage by controlling the frequency or supply voltage subject to a time constraint for minimizing power consumption of MOS transistors.

References

1) James W. Tschanz, James T. Kao, Siva G. Narenda, Raj Nair, Dimitri A. Antoniadis, Anantha P. Chandrakasan and Vivek De, "Adaptive Body Bias for Reducing Impacts of Die-to-Die and Within-Die Parameter Variations on Microprocessor Frequency and Leakage," IEEE J. Solid-State Circuits, vol. 37, pp.1396-1402, (Nov. 2002).

2) T.Kuroda, T.Fujita, S. Mita, T.Nagamatsu, S.Yoshioka, K.Suzuki, F. Sano, M.Norishima, M.Murota, M.Kako, M.Kinugawa, M. Kakumu, and T. Sakurai, "A 0.9-V, 150-MHz, 10-mW, 4mm^2, 2-D discrete cosine transform core processor with variable threshold-voltage (VT) scheme," IEEE J. Solid-State Circuits, vol. 31, pp.1770-1779, (Nov. 1996).

3) Y. Oowaki, M. Noguchi, S. Takagi, D. Takashima, M. Ono, Y. Matsunaga, K. Sunouchi, H. Kawaguchiya, S.Matsuoka, M. Kamoshida, T. Fuse, A. Watanabe, A. Toriumi, S. Manabe, and A. Hojo,"A sub-0.1μm circuit design with substrate-over-biasing," in IEEE ISSCC Dig. Tech. Papers, pp.88-89, (1998).